

# DATA SHEET

**74F3040**

Dual 4-input NAND 30  $\Omega$  line driver

Product specification  
IC15 Data Handbook

1990 Jan 29

# Dual 4-input NAND 30Ω line driver

# 74F3040

## FEATURES

- 30Ω line driver
- 160mA output drive capability in the Low state
- 67mA output drive capability in the High state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V<sub>CC</sub> and GND when both side pins are used

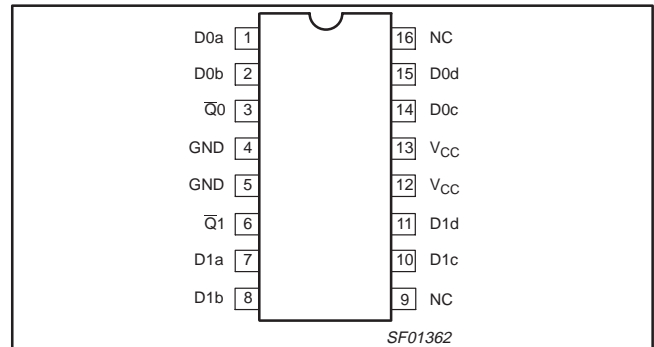
## DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 74F3040 is 67mA source and 160mA sink with a V<sub>CC</sub> as low as 4.5V. This guarantees incident wave switching with V<sub>OH</sub> not less than 2.0V and V<sub>OL</sub> not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	2.0ns	10mA

## ORDERING INFORMATION

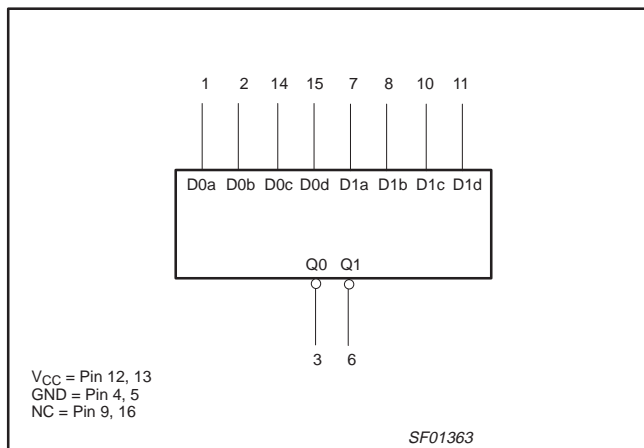
DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F3040N	SOT38-4
16-pin Plastic SOL	N74F3040D	SOT162-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

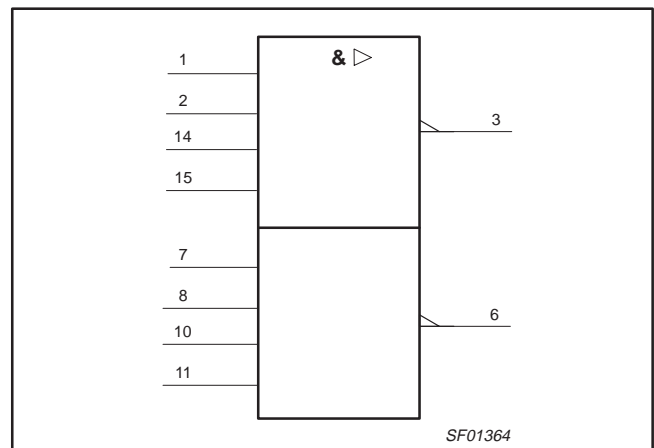
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd	Data inputs	1.0/1.0	20μA/0.6mA
Qn	Data outputs	3350/266	67mA/160mA

**NOTE:** One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



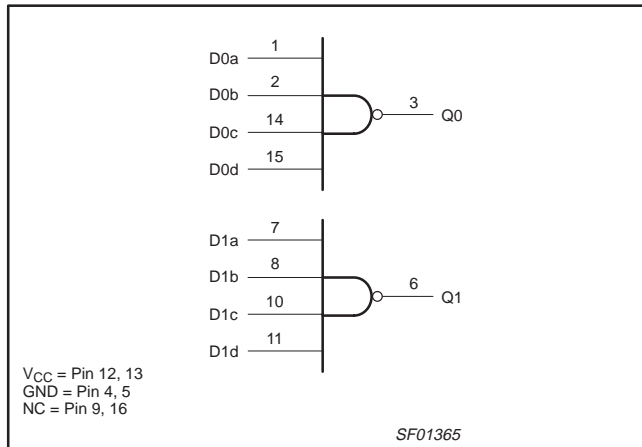
## IEC/IEEE SYMBOL



# Dual 4-input NAND 30Ω line driver

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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\bar{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level  
L = Low voltage level  
X = Don't care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	320	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-67	mA
I <sub>OL</sub>	Low-level output current			160	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT		
				MIN	TYP <sup>2</sup>	MAX			
V <sub>OH</sub>	High-level output current	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OH</sub> = -45mA	±10% V <sub>CC</sub>	2.5			V	
				±5% V <sub>CC</sub>	2.7	3.4		V	
			I <sub>OH1</sub> = -67mA <sup>3</sup>	±10% V <sub>CC</sub>	2.0			V	
V <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OL</sub> = 100mA	±10% V <sub>CC</sub>		0.30	0.50	V	
			I <sub>OL1</sub> = 160mA <sup>4</sup>	±5% V <sub>CC</sub>		0.30	0.50	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2		V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V					100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-0.6	mA	
I <sub>O</sub>	Output current <sup>5</sup>	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25V			-100		-200	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				3.0	5.0	mA
		I <sub>CCL</sub>					16	22	mA

**NOTES:**

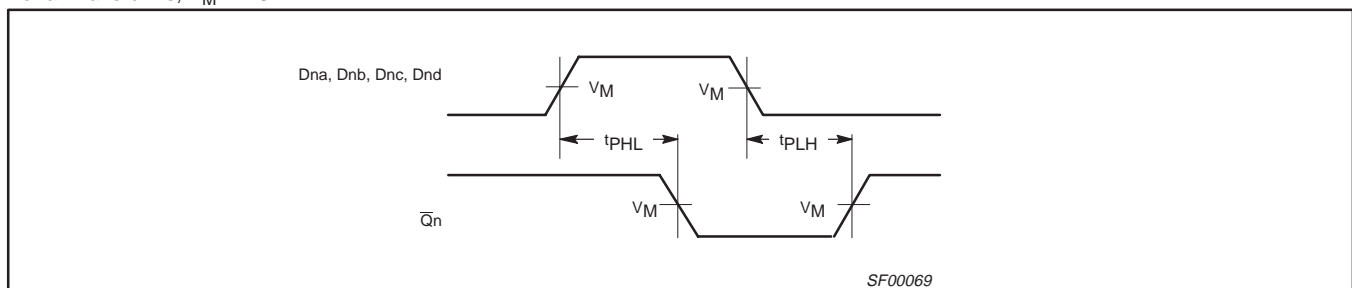
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- I<sub>OH1</sub> is the current necessary to guarantee the Low-to-High transition in a 30Ω transmission line on the incident wave.
- I<sub>OL1</sub> is the current necessary to guarantee the High-to-Low transition in a 30Ω transmission line on the incident wave.
- I<sub>O</sub> is tested under conditions that produce current approximately one half of the true short-circuit output current (I<sub>OS</sub>).

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>na</sub> , D <sub>nb</sub> , D <sub>nc</sub> , D <sub>nd</sub> to $\bar{Q}_n$	Waveform 1	1.0 1.0	2.0 2.0	5.0 4.5	1.0 1.0	5.5 5.0	ns

## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

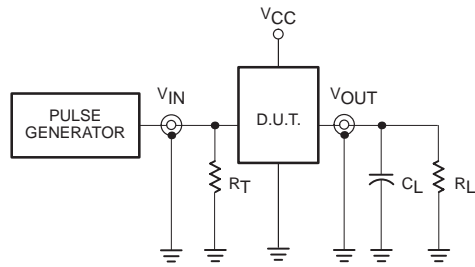


Waveform 1. Propagation Delay for Inputs to Output

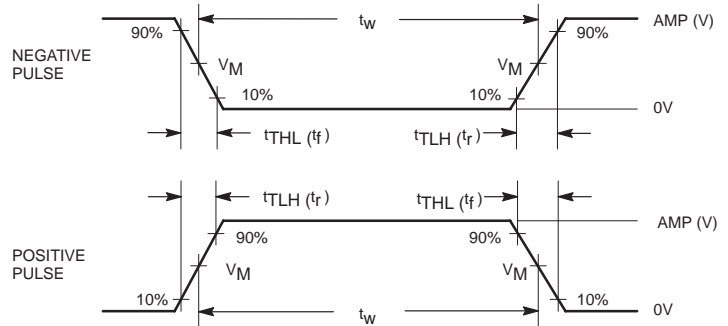
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## TEST CIRCUIT AND WAVEFORMS



**Test Circuit for Totem-Pole Outputs**



**Input Pulse Definition**

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

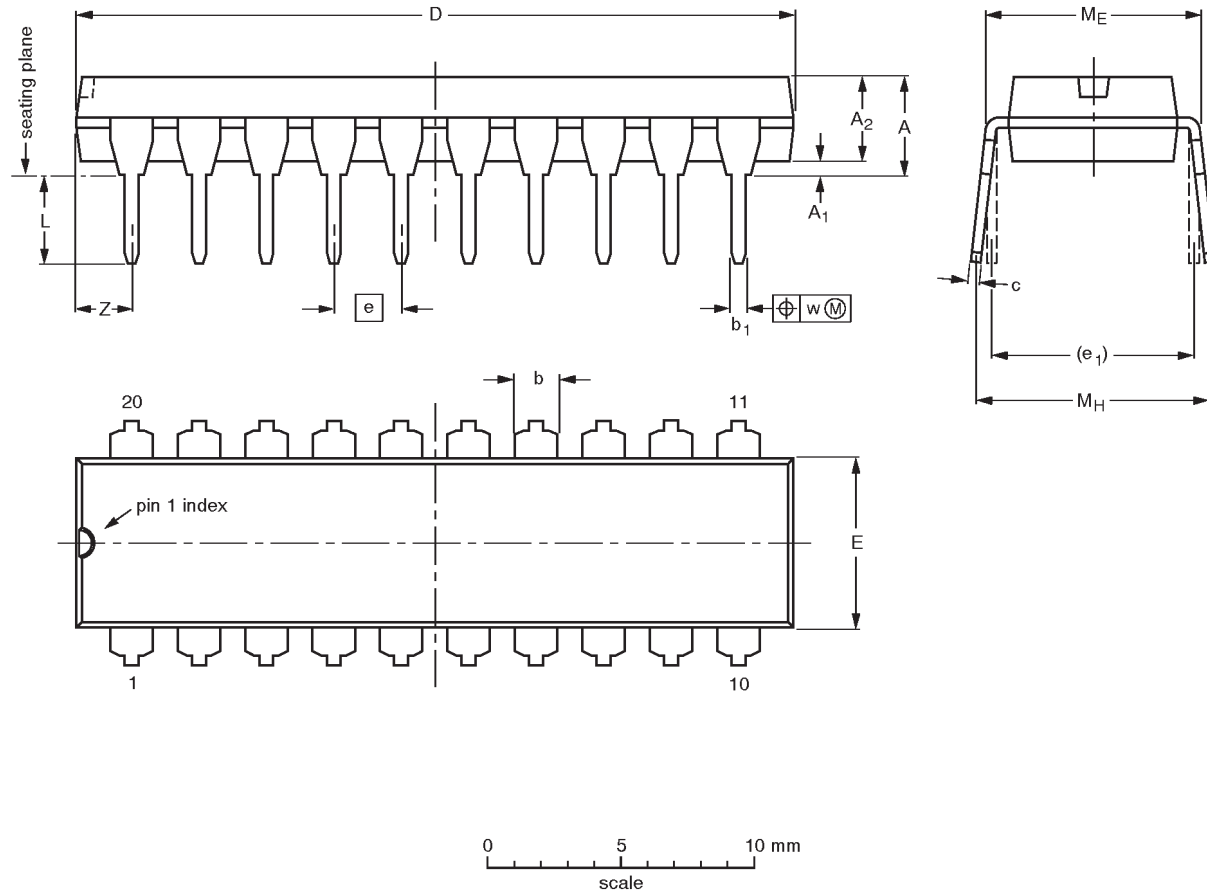
SF00006

# Dual 4-input NAND 30 Ω line driver

## 74F3040

**DIP20: plastic dual in-line package; 20 leads (300 mil)**

**SOT146-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Dual 4-input NAND 30 Ω line driver

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**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

Dual 4-input NAND 30  $\Omega$  line driver

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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